Exhibit 60

UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC, Plaintiff, v. EMC CORPORATION, Defendant.	C.A. No. 1:14-cv-13560-ADB

PLAINTIFF ACQIS, LLC'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

II. PCI BUS TRANSACTIONS, AS DEFINED BY THE PCI STANDARD 3

III. ENCODING OF PCI BUS TRANSACTIONS, AS DESCRIBED AND CLAIMED IN THE ASSERTED PATENTS 4

IV. HISTORY OF "PCI BUS TRANSACTION" CLAIM CONSTRUCTIONS 6

A. Construction of "PCI Bus Transaction" by Judge Davis in the Texas Actions 6

B. Construction of "PCI Bus Transaction" by the PTAB 8

C. Application of the "PCI Bus Transaction" Construction by the PTAB 9

V. HISTORY OF THE CONSTRUCTION OF THE TERM "ENCODED" 12

A. Construction of "Encoded PCI Bus Transaction" by Judge Davis in the Texas Actions 12

B. Construction of the term "Encoded" before the PTAB 13

C. Application of the "Encoded" Construction by the PTAB 14

VI. EMC'S PROPOSED CLAIM CONSTRUCTIONS SHOULD BE REJECTED 15

A. "Peripheral Component Interconnect (PCI) bus transaction" 15

B. "encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms 18

C. "communicating … PCI bus transaction" and related terms 22

VII. CONCLUSION 25

TABLE OF AUTHORITIES

Page(s)

Cases

3M Innovative Properties Co. v. Tredegar Corp.,
725 F.3d 1315 (Fed. Cir. 2013).....16

Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, Inc.,
340 F.3d 1298 (Fed. Cir. 2003).....2

Finisar Corp. v. DirecTV Group, Inc.,
523 F.3d 1323 (Fed. Cir. 2008).....16, 19

Finjan, Inc. v. Secure Computing Corp.,
626 F.3d 1197 (Fed. Cir. 2010).....22

Hill-Rom Servs. v. Stryker Corp.,
755 F.3d 1367 (Fed. Cir. 2014).....8, 16

Kara Tech., Inc. v. Stamps.com Inc.,
582 F.3d 1341 (Fed. Cir. 2009).....17

Markman v. Westview Instruments, Inc.,
517 U.S. 370 (1996).....16

Northern Telecom Ltd. V. Samsung Elecs. Co.,
215 F.3d 1281 (Fed. Cir. 2000).....20

O2 Micro Intern. Ltd. v. Beyond Innov. Tech. Co., Ltd.,
521 F.3d 1351 (Fed. Cir. 2008).....22

Oatey v. IPS Corp.,
514 F.3d 1271 (Fed. Cir. 2008).....17, 23, 24

Perkinelmer, Inc. v. Intema Ltd.,
Case No. 09-10176-FDS, 2011 WL 10756712 (D. Mass. Aug. 12, 2011).....17, 19

Phonometrics, Inc. v. Northern Telecom Inc.,
133 F.3d 1459 (Fed. Cir. 1998).....17

Rexnord Corp. v. Laitram Corp.,
274 F.3d 1336 (Fed. Cir. 2001).....17

Voice Domain Techs., LLC v. Apple Inc.,
Case No. 13-40138-TSH, 2015 WL 4638577 (D. Mass. Aug. 4, 2015)..... *passim*

TABLE OF AUTHORITIES
(continued)

Page(s)

Other Authorities

Decision Denying Institution, Paper 12, Case IPR2014-1452.....6

Joint Notice Regarding Proposed Technical Advisor, D.I. 121, Case No. 6:13-cv-638-LED (E.D. Tex. Dec. 4, 2014).....1

Order Appointing Technical Advisor, D.I. 123, Case No. 6:13-cv-638-LED (E.D. Tex. Dec. 5, 2014).....1

I. INTRODUCTION

Having "gone broad" on construction but failed to invalidate even a single claim before a three-judge panel of the Patent Trial and Appeal Board ("PTAB"), EMC now seeks to improperly narrow the claims to escape infringement. It asks the Court to read physical aspects of the prior art, parallel PCI bus into the claims. That effort would undo two opinions from Judge Davis[1] and the claim constructions adopted and applied by the PTAB.

The constructions of Judge Davis and the PTAB are consistent, well-reasoned, and fully supported by the intrinsic record. Both Judge Davis and the PTAB properly construed the terms "PCI bus transaction" and "encoded." No disavowal, much less clear and unequivocal disavowal, supports altering those constructions or reading unnecessary, additional limitations into well-understood terms such as "communicate," "transmit," "convey," and "output."

EMC's claims that Acqis disavowed claim scope during the IPR proceedings are utterly unfounded. During the PTAB proceedings Acqis repeatedly explained that the prior art, parallel PCI bus has no place in the claims. Acqis further explained that it does not matter how the transactions originate. What matters is that encoded PCI bus transaction information be transmitted over serial interfaces. The PTAB concluded that this did not occur within EMC's prior art.

In contrast to EMC's fictitious assertions, Acqis argued and the PTAB determined that the serial interfaces described in the Horst reference did ***not*** carry encoded PCI bus transactions or ***any bits*** of encoded PCI bus transactions. The reason for this is that the PCI Standard defines a number of transactions used in computer systems, and ***none*** of those transactions was found to

[1] The Court should note that, Judge Davis retained and relied on a technical advisor (proposed by all parties) to assist with claim construction. Order Appointing Technical Advisor, D.I. 123, Case No. 6:13-cv-638-LED (E.D. Tex. Dec. 5, 2014); *see also* Joint Notice Regarding Proposed Technical Advisor, D.I. 121, Case No. 6:13-cv-638-LED (E.D. Tex. Dec. 4, 2014).

be encoded and communicated over the serial interfaces of the Horst system. The PTAB further found that PCI addresses are physical addresses, specifically addresses that map to one of three physical address spaces defined by the PCI Standard, and in utter contrast, the addresses carried over the serial interfaces of the Horst reference were virtual addresses.

The distinctions between the claimed inventions and the Horst reference do ***not*** give EMC any basis to narrow the claims and avoid infringement. The serial PCI Express links in EMC's accused systems carry precisely what Acqis always maintained must be communicated over the recited serial communication links—the accused links carry encoded PCI bus transactions (i.e., the very same transactions defined in the PCI Standard). The PCI Express specification and EMC's own internal documents confirm this fact. Further, the encoded PCI bus transactions communicated over EMC's serial PCI Express links use the very same physical PCI addresses defined in the PCI Standard.

Simply put, the facts here belie EMC's assertions. Incredibly, EMC only offers attorney argument. It offers no technical opinion as to how a person of ordinary skill would interpret the claims or the intrinsic record. There is nothing new to justify reversal of the opinions of Judge Davis and three PTAB judges.

Acqis has consistently maintained that encoded PCI transaction information must be carried over the serial interfaces recited in the claims. That encoded information, however, may be generated directly, for example, by a processor and integrated host interface controller and north bridge, as described with respect to the embodiment of Fig. 8 of the '873 Patent, or it may be generated for purposes of translation, as described with respect to the embodiment of Fig. 6.

Claims should not be construed to eliminate either embodiment from coverage. *Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1308-09 (Fed. Cir. 2003). The

disclosure of the embodiments shows that reading in limitations as EMC asserts would be improper.

II. PCI BUS TRANSACTIONS, AS DEFINED BY THE PCI STANDARD

The PCI Local Bus Specification, cited in the asserted patents, describes several transactions (i.e., information exchanges) that were performed over the prior art, parallel PCI bus. (Brogan Decl.[2], Ex. D at 3 ('873 Patent) (citing PCI Spec.).) The transactions (known to persons of ordinary skill as "PCI bus transactions") allowed a processor and interconnected devices, such as storage, printers, and network connections, to exchange information. The transactions described in the PCI Standard include, among others, memory read and write transactions, I/O read and write transactions, configuration read and write transactions, and interrupt acknowledge transactions. (Lindenstruth Decl. at ¶¶ 61-66.)

As described in the PCI Standard, the information communicated over the course of a transaction typically includes a PCI address (no valid address is sent in an interrupt acknowledge transaction), code identifying a command, and data. (Ex. E at 9, 94 (PCI Spec.).) Software drivers within interconnected devices use the PCI address to determine whether a particular device is the target of a transaction (i.e., whether that device is being asked to do something) and use the coded command data to identify the transaction to be performed (i.e., what is to be done) and the memory space that will be used. (Lindenstruth Decl. at ¶¶ 61-66.)

When communicated over a parallel PCI bus, each transaction "consists of an address phase followed by one or more data phases." (Ex. E at 9 (PCI Spec.).) During the address phase, bytes of a PCI address and bus command are transmitted over the pins and lines of the bus. During the data phase, bytes of data and byte enable information are communicated. (*Id.*;

[2] All exhibits cited refer to the exhibits attached to the Declaration of James Brogan, unless otherwise noted.

(Lindenstruth Decl. at ¶ 63.)

PCI bus transactions (i.e., information communicated in accordance with the PCI Standard) are separate and distinct from the physical, parallel interconnect circuitry used for the communication. (Lindenstruth Decl. at ¶¶ 63, 79-88.) To a person of ordinary skill in the art, transactions represent one layer of a communication protocol, and the physical, parallel communications infrastructure circuitry represents a different, distinct layer of the protocol. (*Id.*)

III. ENCODING OF PCI BUS TRANSACTIONS, AS DESCRIBED AND CLAIMED IN THE ASSERTED PATENTS

When developing his inventions, Dr. Chu chose to keep the information contained in the transaction layer of the PCI protocol, but eliminate the physical layer of that protocol and instead switch to a serial communication architecture. (Ex. D at 4:50-58 ('873 Patent); Lindenstruth Decl. at ¶¶ 43-48; Chu Decl. at ¶ 6.) Dr. Chu recognized that his serial architecture had several uses. It could provide communication between conventional PCI buses, or it could provide communication directly between components, eliminating the need for an intervening PCI bus. (Chu Decl. at ¶¶ 7-10; Lindenstruth Decl. at ¶¶ 60, 107-110.) Figure 8 of the '873 patent illustrates the latter embodiment. (Ex. D at Fig. 8; Lindenstruth Decl. at ¶¶ 107-108.)

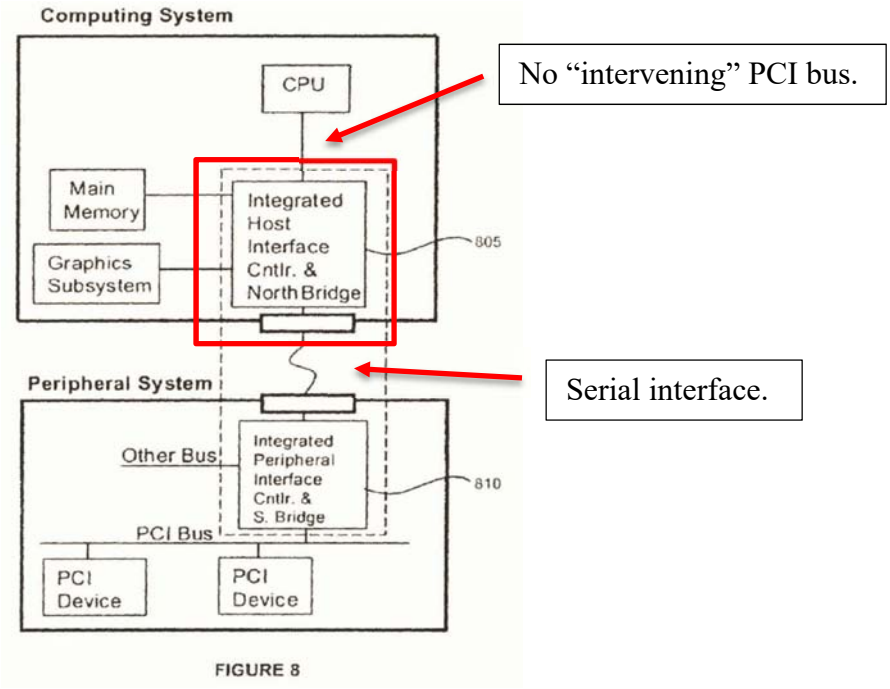

FIGURE 8

As shown in Fig. 8, the Integrated Host Interface Controller and North Bridge 805 of the computing system takes PCI transaction information, as defined by the PCI specification, and encodes that information for transmission over the serial LVDS interface. No PCI bus is required to create the content, because the content is defined by the PCI Standard, and the generation of that content by processors and other devices within computer systems was well known at the time. (Lindenstruth Decl. at ¶¶ 60, 144.)

As described in the patent specification, PCI bus transaction information (i.e., address, command, and data information in accordance with the PCI Standard) is packetized into specific sized packets and ordered for transmission on one or more serial LVDS channels. (Ex. D at 6:34-35, 20:27-48 ('873 Patent); Lindenstruth Decl. at ¶¶ 41-48.) Figure 15 of the '873 Patent provides an illustration of a set of LVDS channels that make up a serial interface for carrying

packetized PCI bus transaction information. (Ex. D at Fig. 15 ('873 Patent)[3]; Lindenstruth Decl. at ¶ 43.) The PCI transaction information is packetized and distributed across the LVDS channels for transmission. (Ex. D at 6:34-35, 20:27-48 ('873 Patent); Lindenstruth Decl. at ¶¶ 41-48.) In such an embodiment, the complete PCI bus transaction would not travel across any single LVDS channel, but rather, would be distributed across the set of channels. (Ex. D at Fig. 15, 21:32-35 ('873 Patent); Lindenstruth Decl. at ¶¶ 43-45.)

Consistent with the embodiment of Fig. 8, several asserted claims expressly recite that the encoded (i.e., packetized and ordered) PCI bus transactions are produced "without an intervening PCI bus."[4] Claim 24 of the '171 Patent[5], reproduced in relevant part below, is exemplary.

> 24. A method Comprising:
> providing a computer module, the module comprising
> a processor unit,
> a connection program,
> an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit coupled to the central processing unit **without any intervening PCI bus**, and
> a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction….

IV. HISTORY OF "PCI BUS TRANSACTION" CLAIM CONSTRUCTIONS

A. Construction of "PCI Bus Transaction" by Judge Davis in the Texas Actions

Judge Davis first addressed the term "PCI Bus transaction" in the Acqis trial with IBM. (Ex. T at 7-11 (Acqis I Second Claim Const. Order).) IBM's expert argued that the term "PCI

---

[3] *See also* Ex. V at Fig. 17 ('814 Patent); Ex. Y at Fig. 11 ('119 Patent); Ex. W at Fig. 16 ('984 Patent); Ex. X at Fig. 11 ('171 Patent) at Fig. 11; Ex. M at Fig. 16 ('468 Patent); '416 Patent at Fig. 15; '624 Patent at Fig. 15; '487 Patent at Fig. 15; '294 Patent at Fig. 12; '961 Patent at Fig. 11.

[4] *See also* Ex. X at claim 24 ('171 Patent); Ex. V at claim 31 ('814 Patent); Ex. W at claims 48, 85 ('984 Patent); Ex. Y claims 38 and 39 ('119 Patent).

[5] EMC requested *Inter Partes Review* of the '171 Patent, but the PTAB denied institution. Ex. GG at 19 (Decision Denying Institution, Paper 12, Case IPR2014-1452 (P.T.A.B. Mar. 4, 2015).

Bus transaction" required the presence of the actual, parallel, PCI bus. (*Id.* at 9.) Judge Davis took the issue up at the pretrial conference. (*Id.* at 1.) Acqis argued that the term meant "sufficient information to permit decoding to create a PCI bus transaction." (*Id.* at 7.) IBM argued "PCI bus" meant "an industry standard parallel computer bus developed by Intel" where a "bus" is "a set of signal lines to which a number of devices are connected and over which information is transferred between them." (*Id.*) The Court noted "the parties primary dispute is whether the term is limited to the conventional, parallel Local PCI Bus, and, therefore, excludes PCI Express bus architecture and bus protocol." (*Id.*) The Court rejected IBM's position construing the term PCI bus transaction as "a data signal communication with an interconnected peripheral component," reasoning that, "[c]ontrary to IBM's proposal that the 'PCI bus' is 'an industry-standard parallel computer bus developed by Intel,' **the claims and specification are not specifically limited to a traditional, parallel PCI bus**." (*Id.* at 9 (emphasis added).) This reasoning precludes EMC's argument here.

Judge Davis considered the term again at the outset of this litigation, when EMC urged that the term be construed as "signals communicated over a PCI bus," and Acqis urged the term be construed as "digital commands, address, and data information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component." (Ex. U at 8-10 (Texas Court Claim Const. Order).) Judge Davis rejected EMC's definition because the claims and patent specifications make clear that "information in accordance with the PCI Standard can be encoded and conveyed serially without the existence of an originating PCI bus." (*Id.* at 10.) In reaching this conclusion, Judge Davis noted that claim 24 of the '171 Patent states in relevant part:

> 24. A method Comprising:
> providing a computer module, the module comprising

> a processor unit,
> a connection program,
> an integrated interface controller and bridge unit to output an *encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction*, the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus, and
> a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction….

(*Id.* at 9 (emphasis in original).)

The same rationale that precluded reading a physical PCI bus limitation into the claims still applies. Both the claims and specifications of the asserted patents show that information in accordance with the PCI Standard (i.e., content of the described PCI bus transactions) can be encoded and conveyed serially without the existence of an intervening or originating PCI bus. (*See, e.g.*, Ex. V at claim 31, Fig. 18 ('814 Patent)[6]; Lindenstruth Decl. at ¶¶ 60, 98-116.)

B. Construction of "PCI Bus Transaction" by the PTAB

To avoid the force and logic of Judge Davis's reasoning, EMC tries a new argument, claiming that Acqis disavowed claim scope in the IPRs, the alleged disavowal justifying the same narrow construction of "PCI bus transaction" that Judge Davis twice rejected.

Disavowal of claim scope must be clear and unequivocal. *Hill-Rom Servs. v. Stryker Corp.*, 755 F.3d 1367, 1371-72 (Fed. Cir. 2014) ("The standards for finding . . . disavowal are exacting" and require that the history make clear that the invention "is clearly limited to a particular form of the invention."). Nothing in the IPRs supports a factual finding of disavowal.

Importantly, at the outset of the PTAB proceeding, EMC proposed that "PCI Bus transaction" means "a data signal communication with an interconnected peripheral component."

[6] For additional examples include, Ex. D at claim 54 ('873 Patent) (including the limitation "a peripheral bridge directly coupled to the processor."); Ex. W ('984 Patent) at claim 48 (including the limitation "the integrated interface controller and bridge unit directly coupled to the processor without any intervening PCI bus."); Ex. Y ('119 Patent) at claim 38 ("a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus."); Ex. M at claims 30, 37, 45 ('468 Patent).

(Ex. Z at 14-15; Ex. AA at 14-15 (EMC's IPR Petitions).) Taking this position, EMC would have broadened the claims beyond recognition, eliminating any tie to the PCI Bus Standard or to the standard's description of PCI bus transactions.

In Patent Owner's Preliminary Response before the PTAB, Acqis explained that reading the PCI Standard out of the claims would be wrong. Acqis urged, just as it did in district court, that the term "PCI bus transaction" should be construed as "digital command, address, and data information, in accordance with the PCI Standard, for communicating with a peripheral component." (*See, e.g.*, Ex. BB at 4-16; Ex. CC at 4-17 (Acqis's IPR Prelim. Responses).)

The PTAB's Institution Decision applied its own construction of the term, finding that "PCI bus transaction" and "Peripheral Component Interconnect (PCI) bus transaction" mean a "Peripheral Component Interconnect (PCI) industry standard bus transaction." (Ex. Q at 5-7 ('873 Final Written Decision); Ex. R at 5-7 ('814 Final Written Decision).)

Acqis accepted the PTAB's construction of the terms "PCI bus transaction" and "Peripheral Component Interconnect (PCI) bus transaction," as did EMC, although EMC continues on appeal to challenge PTAB's application of that construction.

The constructions of Judge Davis and the PTAB are perfectly consistent. (Lindenstruth Decl. at ¶¶ 98-100.) The PCI Bus Specification defines a set of transactions (memory read, memory write, I/O read, I/O write, etc.) that are communicated over the physical PCI bus structure, and one of those transactions (i.e., information in accordance with the PCI Standard) must be encoded and communicated over the serial interfaces recited in the asserted claims.

C. Application of the "PCI Bus Transaction" Construction by the PTAB

Accepting the PTAB's construction of the terms "PCI bus transaction" and "Peripheral Component Interconnect (PCI) bus transaction" as a "Peripheral Component Interconnect industry standard bus transaction," Acqis and its expert, Dr. Volker Lindenstruth, explained to

the PTAB: (1) how PCI bus transactions are defined within the PCI Standard; (2) how those transactions are encoded and transmitted over the serial, LVDS channels in the claimed invention; (3) how those transactions are encoded and transmitted over serial, LVDS channels within the context of the accused PCI Express links; and (4) why no encoded PCI Standard bus transactions are carried over the serial, LVDS links of the Horst and Bogaerts prior art references. (Ex. A at ¶¶ 60-117 ('873 Lindenstruth IPR Decl.); Ex. B at ¶¶ 59-75 ('814 Lindenstruth IPR Decl.).)

Distinguishing the claimed inventions from the systems described in the Horst and Bogaerts references, Dr. Lindenstruth explained that the traditional PCI bus, PCI Express, and the claimed inventions address fundamentally different problems than those addressed by the Horst and Bogaerts references. (*See, e.g.*, Ex. B at ¶¶ 91, 107.) Specifically, PCI, PCI Express, and the claimed inventions seek to connect a single CPU or CPU node to its local I/O components, whereas the Horst system seeks to connect hundreds of remote processor-memory nodes, each executing its own operating system, with one another and thousands of distributed I/O resources, and the Bogaerts system was designed to allow the sharing of processor and memory resources among distributed computer systems to enable high-speed parallel processing. (*Id.*)

With respect to the Horst system, Dr. Lindenstruth explained that the system was designed to use a completely new protocol, rather than use an existing protocol, such as the PCI protocol. (*Id.* at ¶ 93.) Dr. Lindenstruth further explained that no encoded PCI bus transactions are carried over the serial, LVDS links of the TNet system. (*Id.* at ¶¶ 105-106.) Specifically, the TNet system does not support the memory read, memory write, I/O read, I/O write, configuration read, configuration write, or interrupt acknowledge transactions that are defined by the PCI

Standard and used within PCI buses, PCI express links, and the claimed invention. (*Id.* at ¶ 104.) Nor does the Horst paper disclose any mechanism for the described TNet packets to communicate PCI bus commands indicating a type of PCI bus transaction. (*Id.*) Finally, unlike PCI, PCI Express, and the claimed inventions, which all use PCI physical addresses, the TNet system used something very different, virtual addresses, and it did that for a reason—if it used physical PCI addresses, the TNet system would not work. (*Id.* at ¶¶ 103-104.)

As for the Bogaerts system, Dr. Lindenstruth explained that the SCI protocol of the Bogaerts system abandons the three flat address spaces required for PCI bus transactions and defines its own, different transaction types. (*Id.* at ¶ 108.) This transaction protocol, like that of Horst, is fundamentally different from the protocols used by PCI, PCI Express, and the claimed inventions.

The PTAB's Final Written Decisions accepted Dr. Lindenstruth's analysis, finding that encoded PCI bus transactions are not communicated over the serial, LVDS links described in the Horst reference. (*See, e.g.,* Ex. Q at 11, 14-15 ('873 Final Written Decision); Ex. R at 10-12, 14-15 ('814 Final Written Decision).) Having determined that EMC failed to establish Bogaerts as a prior art printed publication, the PTAB did not address the technical aspects of Bogaerts. (Ex. R at 17-20.)

As for EMC's unfounded accusations of inconsistent position taking, Acqis directs the Courts attention to pages 46-50 of the hearing transcript. There, counsel for Acqis, Mr. Stacy, explains that the claims at issue **do not require a conventional PCI bus**. (*See, e.g.,* Ex. P at 46:11-22, 47:9-48:12 (P.T.A.B. Dec. 8, 2015 Trial Tr.).) The questions and answers below are particularly relevant.

> JUDGE TIERNEY: So can you relate that information that we just discussed that is on the CPU side there's no PCI bus with Figure 8 of your patent

in the '873 patent?

MR. STACY: So on Figure 8 of the '873 patent, you have to look at the text. It's talking about a PCI transaction. **And so the claims don't require a bus. They require a PCI transaction to take place.** You are looking at the standard the whole time. I'm putting a transaction together that looks like a PCI transaction. **So all of my PC[I]-compliant drivers know how to read it. So I have created my PCI transaction. That's why it matters, my drivers can read it.**

* * *

JUDGE WEINSCHENK: Can you explain to me again how we know in Horst that the CPU doesn't start with a PCI transaction and scramble it into TNet and then re-unscramble it to a PCI? So the lack of a PCI bus is not determinative is what I'm hearing you say.

MR. STACY: **That's correct. The lack of a PCI bus is indicative but not determinative.** In this particular instance they have been able to point to nothing that shows that there's a PCI transaction ever generated….

(*Id.* at 46:11-21, 47:19-48:2 (emphasis added).)

Far from asserting that a PCI bus must be present, Mr. Stacy took precisely the opposite position, stating that the claims do not require a PCI bus. They require a transaction defined by the PCI Standard (i.e., memory read, memory write, I/O read, I/O write, etc.) to take place. (Lindenstruth Decl. at ¶¶ 117-126, 137-145.) Mr. Stacy went on to explain that, while the presence of a PCI bus is indicative of whether an encoded PCI bus transaction may be present, it is not determinative. (Ex. P at 47:22-25.) The point is that something must create the transaction content, and then that content must be communicated over the serial, LVDS channel. The delivered PCI bus transaction content is then used by PCI-compliant software drivers to effect the transactions. As Mr. Stacy explained, a prior art, PCI bus need not be present to do this. (*Id.* at 46:14-48:2; Lindenstruth Decl. at ¶¶ 137-145.)

V. HISTORY OF THE CONSTRUCTION OF THE TERM "ENCODED"

A. Construction of "Encoded PCI Bus Transaction" by Judge Davis in the Texas Actions

Just as Judge Davis considered and rejected EMC's attempt to read a physical PCI bus limitation into the term "PCI bus transaction," Judge Davis considered and rejected EMC's

attempt to make parallel-to-serial conversion a requirement for encoding. (Ex. U at 10-11 (Texas Claim Const. Order).) Judge Davis construed "encoded PCI bus transaction" as "code representing a PCI bus transaction." (*Id.*) As Judge Davis recognized, "the claim language suggests that an encoded PCI bus transaction does not require any parallel-to-serial conversion at all." (*Id.* at 11.) Judge Davis also noted that such a reading is supported by the patent specifications. (*Id.* at 11 (citing '873 Patent at 5:34–48).)

B. Construction of the term "Encoded" before the PTAB

The term "encoded" was specifically addressed as part of the PTAB proceedings. Dr. Lindenstruth opined that the patent specifications describe three types of encoding: (1) turning signals into bits; (2) packetizing bits into a specified size packet; and (3) ordering bits onto one or more serial transmission lines. (Ex. A at ¶ 125; *see also id.* at ¶¶ 121-124 ('873 Lindenstruth IPR Decl.); Ex. B at ¶ 120; *see also id.* at ¶¶ 116-119 ('814 Lindenstruth IPR Decl.).) Consistent with Judge Davis's construction, two of these three types of encoding (packetizing bits into a specified size packet and ordering bits onto one or more serial transmission lines) do not require any form of parallel-to-serial conversion. (Lindenstruth Decl. at ¶ 123.) Rather, they address preparing data for transmission over a serial interface. (Lindenstruth Decl. at ¶¶ 120-121.)

At the hearing, Mr. Stacy explained that it does not matter where a transaction may originate (e.g., whether on a parallel bus or within a memory register); what matters is what is communicated over the serial bus:

> MR. STACY: I would quarrel with any indication that we said it had to originate. I'm not sure what originate means. In this instance, what that claim requires is that it is a PCI bus transaction. That is defined by the standard. You know the three portions: Address, data and control. And you have to take that, whatever that would be in parallel form and you are going to encoded it, encode a serial bit stream. **So, I'm taking the transaction data, I don't think that it matters where it originates from, then I'm going to take it, I'm going to serialize it and then send it out over my serial bus for speed purposes.** That's why you are doing all of this.

(Ex. P at 50:12-22 (P.T.A.B. Dec. 8, 2015 Trial Tr.) (emphasis added).) This statement and others like it do not disavow anything. To the contrary, they are perfectly consistent with the constructions of Judge Davis and the PTAB. (Lindenstruth Decl. at ¶ 124.) What counts in the context of the claims is that PCI transaction data is packetized and ordered for transmission over the serial transmission lines. (Lindenstruth Decl. at ¶¶ 120-122.)

C. Application of the "Encoded" Construction by the PTAB

Consistent with the definition of the term "encoded" provided by Dr. Lindenstruth, and consistent with Mr. Stacy's statements at the hearing, the PTAB's Final Written Decision focuses on the information communicated over serial interfaces, and not on where or how that information originated. (Lindenstruth Decl. at ¶¶ 146-153.) For example, at page 12 of its decision concerning the '814 patent, the PTAB states:

> But claims 24 and 31 require more than just communicating information over the serial channels that might be used in the console to create a PCI bus transaction. Claims 24 and 31, when read in light of the specification, **require that the information actually communicated over the serial channels includes address and data bits of a PCI industry standard bus transaction in serial form** … As discussed above, the evidence identified in the Petition does not indicate that the information output by the TNet processor over the TNet links includes address and data bits of a PCI Industry standard bus transaction in serial form.

(Ex. R at 12 ('814 Final Written Decision) (emphasis added) (citations omitted).)

This analysis, following the testimony of Dr. Lindenstruth and the argument presented by Mr. Stacy at the hearing, evidences no disavowal of claim scope. The PTAB reached a similar conclusion regarding the output of the TNet bus interface:

> Specifically, Petitioner argues that "the PCI device creates a PCI bus transaction, which is then serialized to be communicated over the TNet channel." … Petitioner's argument and evidence are not persuasive. **Horst teaches that the TNet bus interface translates an I/O bus transaction, such as a PCI bus transaction, into a TNet transaction, *before* the transaction is encoded for serial communication over the TNet links … As a result, the TNet bus interface outputs a TNet virtual address in serial form, not address bits of a PCI industry standard bus transaction in serial form**.

(*Id.* at 15 (emphasis added) (citations omitted).)

Here again, the PTAB focused on the content output onto the serial interface, and not where that content originated or whether it came from parallel-to-serial conversion. (Lindenstruth Decl. at ¶¶ 146-153.) This, again, is perfectly consistent with Judge Davis's treatment of the term "encoded." (Ex. U at 11 (Texas Claim Const. Order; Lindenstruth Decl. at ¶ 124).)

VI. EMC'S PROPOSED CLAIM CONSTRUCTIONS SHOULD BE REJECTED

A. "Peripheral Component Interconnect (PCI) bus transaction"

Acqis's proposed construction	EMC's proposed construction
"information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component" In the alternative, "a transaction, in accordance with the PCI Standard, for communicating with an interconnected peripheral component."	"a transaction, as defined by the industry standard PCI Local Bus Specification, involving a PCI bus"

This Court should construe "PCI bus transaction" consistently with the constructions adopted and applied by Judge Davis and the PTAB, both of which are supported by the intrinsic record, and neither of which incorporates the prior art, parallel PCI bus. Properly construed, the term means "information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component." EMC provides no basis for deviating from this construction.

As Judge Davis properly concluded, the claims at issue and the patent specifications make clear that "information in accordance with the PCI Standard can be encoded and conveyed serially without the existence of an originating PCI bus." (Ex. U at 10 (Texas Claim Const. Order).) This is readily apparent from the clear language of the asserted claims and the embodiment of Fig. 8, which provides for encoding of PCI bus transactions without an

intervening PCI bus.[7] (Ex. D at Fig. 8; *see also* Ex. M at Fig. 20; Lindenstruth Decl. at ¶¶ 107-110.) The PTAB's construction of PCI bus transaction is perfectly consistent with this.

EMC's evidence of claimed disavowal is not persuasive. At the PTAB hearing, Acqis's counsel stated that the claims "do not require a PCI bus." (Ex. P at 46:6-7 (P.T.A.B. Dec. 8, 2015 Trial Tr.); *see also id.* at 47:24-25; Lindenstruth Decl. at ¶¶ 137-145.) This is the opposite of disavowal, particularly here where the standards are "exacting." *See, e.g., Voice Domain Techs., LLC v. Apple Inc.*, Case No. 13-40138-TSH, 2015 WL 4638577, at *3, *16 (D. Mass. Aug. 4, 2015) (quoting *3M Innovative Properties Co. v. Tredegar Corp.*, 725 F.3d 1315, 1322 (Fed. Cir. 2013)); *Hill-Rom*, 755 F.3d at 1371-72 ("The standards for finding . . . disavowal are exacting.").

The claims require that an encoded PCI bus transaction (i.e., encoded information in accordance with the PCI Standard) be communicated on the recited serial interfaces. (*See, e.g.*, Ex. D at claim 54 ('873 Patent).) The claims do not require a parallel PCI bus, or that a transaction be produced by a parallel PCI bus. (*See id.*; *see also* Lindenstruth Decl. at ¶¶ 98-116, 137-145.) Acqis made this very clear to the PTAB, and the PTAB applied the PCI bus transaction limitations accordingly.

In view of this clear evidence, the Court should follow Judge Davis's construction. The Federal Circuit has repeatedly confirmed "'the importance of uniformity in the treatment of a given patent,'" and EMC's claim construction brief provides no justification for upsetting Judge Davis's construction. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1329 (Fed. Cir. 2008) (quoting *Markman v. Westview Instruments, Inc.*, 517 U.S. 370 (1996)); *see also*

[7] *See, e.g.*, Ex. W ('984 Patent) at claim 48 (including the limitation "the integrated interface controller and bridge unit directly coupled to the processor without any intervening PCI bus."); Ex. X ('171 Patent) at claim 24 (including the limitation "the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus."); Ex. Y ('119 Patent) at claim 38 (including the limitation "a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus."); Ex. D at claim 54 ('873 Patent) (including the limitation "a peripheral bridge directly coupled to the processor.").

Perkinelmer, Inc. v. Intema Ltd., Case No. 09-10176-FDS, 2011 WL 10756712, at *6-7 (D. Mass. Aug. 12, 2011; *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001); *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1465 (Fed. Cir. 1998).

As for EMC's assertion that Acqis seeks to read the concept of a "transaction" out of the claims, that argument is completely unfounded. (Op. Br. at 10-11, D.I. 185.) PCI bus transactions are precisely the "information in accordance with the PCI Standard" that must be encoded and communicated over the recited serial interfaces. (Ex. U at 10 (Texas Claim Const. Order).) Accordingly, should the Court substitute the word "transaction" for "information" in Judge Davis's construction, Acqis would have no objection to that.

EMC's position contradicts the express language of several asserted claims and excludes the preferred computer system of Fig. 8 from coverage. For these reasons, the Court should reject it. *See, e.g., Oatey v. IPS Corp.*, 514 F.3d 1271, 1276-77 (Fed. Cir. 2008) ("We normally do not interpret claim terms in a way that excludes embodiments disclosed in the specification."); *see also Kara Tech., Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009).

The fundamental illogic of EMC's proposed construction can be seen by applying it to claim 24 of the '171 patent; using EMC's proposal claim 24 would read in relevant part:

> "an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of [a transaction, as defined by the industry standard PCI Local Bus Specification, **involving a PCI bus**], the integrated interface controller and bridge unit coupled to the central processing unit **without any intervening PCI bus**."

(Ex. X at claim 24 (emphasis added).) In this example, claim 24 would require involving a PCI bus to output the encoded serial bit stream of PCI bus transaction, and in the next breath, impossibly exclude that same PCI bus. EMC's construction would exclude the embodiment disclosed in Figure 8 and is, therefore, incorrect. *See, e.g., Oatey*, 514 F.3d at 1276-77. Based on

the language of the claims, it is clear that the "encoded serial bit stream of PCI bus transaction" refers to the ***information*** output over the serial channel, and not the type of physical structure used to produce or carry that information. EMC illogically conflates the two issues, and that would be error.

B. "encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms[8]

Acqis's proposed construction	EMC's proposed construction
"encoded … PCI bus transaction" means "code representing a PCI bus transaction"	"a PCI bus transaction that has been serialized from its original parallel format"

Like "PCI bus transaction," the Court should construe "encoded" consistently with the constructions adopted and applied by Judge Davis and the PTAB. The intrinsic record plainly supports those constructions, and neither Judge Davis nor the PTAB judges incorporated a parallel-to-serial conversion requirement into the construction. (Ex. U at 11 (Texas Claim Const. Order); Ex. D at 5:34-38, 17:54-60, 21:65-67, 21:61-65, 16:55-58, 17:11-13, Figs. 13-15; Lindenstruth Decl. at ¶¶ 117-126.)

Judge Davis construed the term "encoding" to mean "assigning code to represent data for a bus transaction," rejecting EMC's first attempt to read parallel-to-serial conversion into the claims. The intrinsic record supports Judge Davis's construction. (Ex. U at 11 (Texas Claim Const. Order) (citing '873 Patent at 5:34-48).) The claims cover only what is communicated over the serial channel—encoded PCI bus transaction information—and not the origin of what is communicated. (Section VI(A), above.) That is perfectly consistent with both the positions Acqis took before the PTAB and the ultimate treatment of the term "encoded" by the PTAB. (Section V(B)-(C) above.) In short, the proceedings before the PTAB fully support Judge

[8] The parties previously agreed on the meaning of the terms "serial bit channel," "serial … channel," "channels … to transmit … as serial data" and "serial bit stream." (Ex. U at 32 (Texas Claim Const. Order).)

Davis's construction, and no clear and unequivocal disavowal mandates a change. Maintaining consistency in claim construction also weighs in favor of adopting Judge Davis's construction. *Finisar*, 523 F.3d at 1329; *Perkinelmer*, 2011 WL 10756712, at *6-7.

EMC's proposal improperly reads limitations into the claims. Judge Davis addressed this very issue in Texas, finding that (1) the specifications do not tether "encoding" to parallel-to-serial conversion, and (2) the "claim language suggests that an encoded PCI bus transaction does not require any parallel-to-serial conversion at all." (Ex. U at 11 (Texas Claim Const. Order).) In fact, many claims specifically recite the generation and communication of encoded PCI bus transaction information "without an intervening PCI bus."[9]

The PTAB construed the term "encoded" consistent with Judge Davis's construction. Dr. Lindenstruth testified that the patent specifications describe three specific types of encoding: (1) turning signals into bits; (2) packetizing bits into a specified size packet; and (3) ordering bits onto one or more serial transmission lines. (Ex. A at ¶ 125, *see also id.* at ¶¶ 121-124 ('873 Lindenstruth IPR Decl.); Ex. B at ¶ 120, *see also id.* at ¶¶ 116-119 ('814 Lindenstruth IPR Decl.).) Consistent with Judge Davis's construction, two of these three types of encoding (packetizing bits into a specified size packet and ordering bits onto one or more serial transmission lines) do not require any form of parallel-to-serial conversion. (Lindenstruth Decl. at ¶¶ 122-123.) The PTAB focused on the content of the information carried over the serial TNet interfaces, and not how that content originated. Highlighting this point, the PTAB rejected EMC's assertion that, because the TNet Bus Interfaces described in Horst communicated with

[9] *See, e.g.*, Ex. W ('984 Patent) at claim 48 (including the limitation "the integrated interface controller and bridge unit directly coupled to the processor without any intervening PCI bus."); Ex. X ('171 Patent) at claim 24 (including the limitation "the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus."); Ex. Y ('119 Patent) at claim 38 (including the limitation "a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus."); Ex. D at claim 54 ('873 Patent) (including the limitation "a peripheral bridge directly coupled to the processor.").

devices over a PCI bus, those TNet Bus Interfaces must inherently output encoded PCI bus transactions over the described serial TNet links. The PTAB rejected EMC's position, because "the TNet bus interface translates an I/O bus transaction, such as a PCI bus transaction, into a TNet transaction, *before* the transaction is encoded for serial communication over the TNet links … As a result, the TNet bus interface outputs a TNet virtual address in serial form, not address bits of a PCI industry standard bus transaction in serial form." (Ex. Q at 15 n.4 ('873 Final Written Decision) (emphasis in original); *see also* Ex. R at 15 ('814 Final Written Decision).) For the PTAB, the proper focus was on the information communicated over the serial links, not where or how that information came to exist.

During the IPR proceedings, Acqis never took the position that encoding required parallel-to-serial conversion. Such a position would contradict the very definition of "encoding" proffered by Dr. Lindenstruth. (Ex. DD at 18-20 ('873 Patent Owner's Response); Ex. A at ¶ 125, *see also id.* at ¶¶ 121-124 ('873 Lindenstruth IPR Decl.).) EMC offers sound bites from the PTAB trial transcript that are misleading. When the complete IPR record is considered, Acqis's arguments do not come close to the "clear and unmistakable" disavowal required to narrow the term "encoded" from its ordinary meaning. *Voice Domain* Techs, 2015 WL 4638577, at *3; *see Northern Telecom Ltd. V. Samsung Elecs. Co.*, 215 F.3d 1281, 1294 (Fed. Cir. 2000) (refusing to narrow a claim term or exclude particular embodiments where the court "simply cannot tell" if the inventor intended any exclusion).

Furthermore, the parallel-to-serial discussion before the PTAB sprung from the fact that the prior art references presented by EMC included proprietary serial communication links and a prior art, parallel PCI bus. (Ex. Q at 8-9 (showing Horst with PCI bus); Ex. R. at 8-10 (same); Lindenstruth Decl. at ¶¶ 146-153.) The PTAB did not distinguish Acqis's patents from the prior

art based on a lack of parallel-to-serial conversion; the PTAB determined that the prior art failed to disclose communicating an encoded PCI bus transaction over a serial channel. (*Id.*; Ex. Q, at 14, 15 n.4 ('873 Final Written Decision); Ex. R at 14-15 ('814 Final Written Decision).) For this reason as well, EMC's argument, that Acqis limited the scope of "encoded" through its arguments before the PTAB, should be rejected.

To support its argument, EMC references a statement in Acqis's Patent Owner Response, "***one key*** to the invention was to serialize the otherwise parallel PCI bus transactions." (Op. Br. at 19, D.I. 185 (citing Ex. 5 at 3) (emphasis added).) That statement addresses the need to abandon the prior art parallel, physical layer and move to a serial physical layer. Incredibly, EMC omits the all-important sentence that follows: "***Another key*** was to maintain the PCI transaction address bits as generated on the CPU side of the network so that the serialized communications were compatible with existing peripheral devices and their drivers." (*Id.* (emphasis added).) Acqis's description of the "keys" to the invention simply do not require limiting encoding to parallel-to-serial conversion. *Voice Domain Techs.*, 2015 WL 4638577, at *3.

While Acqis discussed various embodiments before the PTAB, including embodiments describing parallel-to-serial conversion, there was no disavowal of claim scope. For example, EMC argues that Acqis's statement: "And the point is you take it from parallel to serial and back to parallel," necessarily limits "encoded" to EMC's construction. (Op. Br. at 19, D.I. 185.) EMC's argument utterly ignores that Acqis's counsel confirmed that the claims do not require a parallel, PCI bus, and the focus must be on the content carried over the serial interface:

> JUDGE TIERNEY: So can you relate that information that we just discussed that is on the CPU side there's no PCI bus with Figure 8 of your patent in the '873 patent?
>
> MR. STACY: So on Figure 8 of the '873 patent, you have to look at the

> text. It's talking about a PCI transaction. **And so the claims don't require a bus.** They require a **PCI transaction to take place**. You are looking at the standard the whole time. **I'm putting a transaction together that looks like a PCI transaction. So all of my PCS-compliant drivers know how to read it**. So I have created my PCI transaction. That's why it matters, my drivers can read it. And then I'm taking it at a parallel form, putting it into serial form and then back to parallel. **The point about Horst is that Horst doesn't have a PCI transaction that is then serialized**. **And one indicator is that there's no PCI bus but it makes no difference whether there is.**

(Ex. P at 46:11-25 (P.T.A.B. Dec. 8, 2015 Trial Tr.); *see also id.* 47:24-48:2, 50:18-22.) This statement alone is fatal to EMC's position and illustrates the misleading characterization of snippets of the IPR record. *Voice Domain Techs.*, 2015 WL 4638577, at *3. (Lindenstruth Decl. at ¶¶ 137-145.)

In sum, EMC failed to prove Acqis made clear and binding statements in the IPR that would require reversing constructions from three PTAB judges and Judge Davis.

C. "communicating … PCI bus transaction" and related terms

Acqis's proposed construction	EMC's proposed construction
"communicating," "communicate," "transmitting," "transmit," "convey," and "output," are terms that are easily understood by a lay person and need no construction.	"communicating a PCI bus transaction, including all address, data, and control bits, without discarding any of those bits"

The Court should not construe a claim if its ordinary meaning is readily understood by a layperson. *See O2 Micro Intern. Ltd. v. Beyond Innov. Tech. Co., Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008); *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1206-07 (Fed. Cir. 2010). When read in view of the claims and specification, "communicating," "communicate," "transmitting," "transmit," "convey," and "output," require no construction. Furthermore, Acqis's positions before the PTAB do not narrow the scope of the claims as EMC argues.

Once the Court resolves the parties' dispute regarding "PCI bus transaction," construction of "communicating … PCI bus transaction" and related terms will be unnecessary. The parties do not dispute that "PCI bus transaction" is a transaction defined by the PCI Standard. (Section

VI(A), above). "Communicating … PCI bus transaction," therefore must refer to communicating a transaction or information in accordance with the PCI Standard.

EMC's proposed construction contradicts several asserted claims, which require the communication of "address and data bits of PCI bus transaction" without referencing other information, such as PCI command codes. (*See, e.g.*, Ex. X at claim 24 ('171 Patent); Lindenstruth Decl. at ¶ 129.)

Further, EMC's proposed construction, in the context of the claim language, may be read to require that all bits of a PCI bus transaction be sent across a single LVDS channel. However, as is shown in Figure 15 of the '873 Patent, bits of a single PCI bus transaction can be broken up and sent across multiple LVDS channels. (Ex. D, Fig. 15; *see also id.* at 20:44-47 ("The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3::0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#."), 21:32-33 ("Fig. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in Figs. 13 and 14 from the HIC to the PCI."); Lindenstruth Decl. at ¶ 132.) EMC's proposed construction could improperly exclude the embodiment of Figure 15.[10] *Oatey*, 514 F.3d at 1276-77.

EMC's construction also implies that all bits of a PCI bus transaction must be communicated simultaneously, but that does not happen in memory read, I/O read, or configuration read transactions, where a command requesting information is sent to a device and, in response, the device returns the requested data. In such transactions, the encoded command and address information would be transmitted over a set of LVDS channels that communicate

[10] Figure 15 is cited in all of the Acqis patents, '814 Patent at Fig. 17; '416 Patent at Fig. 15; '624 Patent at Fig. 15; '487 Patent at Fig. 15; '294 Patent at Fig. 12; '961 Patent at Fig. 11; '984 Patent at Fig. 16; '119 Patent at Fig. 11; '171 Patent at Fig. 11; '468 Patent at Fig. 16.

data in one direction, and the requested data would be returned over a different set of LVDS channels that communicate data in the opposite direction.

As for EMC's disavowal arguments, while Acqis explained and the PTAB found that a physical PCI address must be included within a PCI bus transaction, Acqis did not argue that the entire address must be communicated over a single LVDS channel, because the claimed serial interfaces include multiple LVDS channels. (*See, e.g.*, Ex. D at Fig. 15; Ex. P at 35:19-23 (P.T.A.B. Dec. 8, 2015 Trial Tr.); Lindenstruth Decl. at ¶¶ 132-133.) Similarly, while Acqis explained and the PTAB found that a PCI bus transaction includes code for defining the type of transaction, Acqis never indicated that the entire code must be sent across a single LVDS channel. (*Id.*) Such requirements would exclude the embodiment of Fig. 15 from coverage and are presumed improper. *Oatey*, 514 F.3d at 1276-77.

EMC spends the majority of its argument claiming that Acqis's statements to the PTAB require adopting its construction. (Op. Br. at 22-25, D.I. 185.) As with "PCI bus transaction" and "encoded," EMC's portrait of the IPR proceedings is misleading and inaccurate. Acqis's statements do not rise to the "clear and unmistakable" disavowal required to narrow the claim term from its ordinary meaning. *Voice Domain*, 2015 WL 4638577, at *3.

Highlighting a significant challenge with EMC's proposal, that proposal would exclude interrupt acknowledge transactions, as defined in the PCI Standard, from coverage. As counsel for Acqis explained at the PTAB hearing:

> In an interrupt acknowledge, the address is zeroed out. It's null. So if you look at ['873 patent] claim 54, it says all PCI bus transactions. That covers everything. What does ['873 patent] claim 61 do? Claim 61 narrows it and says this PCI transaction has to have encoded PCI address and data bits."

(Ex. P at 35:19-23 (P.T.A.B. Dec. 8, 2015 Trial Tr.).) By requiring all address bits, EMC's proposed construction would exclude this type of PCI bus transaction from the claims, or at the

very least cause severe jury confusion. (Lindenstruth Decl. at ¶¶ 130-133.)

The PTAB did not distinguish the prior art based on its lack of communicating "all address, data, and control bits, without discarding any of those bits." In fact, the PTAB found that Horst did not anticipate the challenged patents because it did not disclose "that *any* bits of a PCI industry standard bus transaction are included in the TNet transaction output by the TNet processor interface," and that "the TNet bus interface outputs a TNet transaction that has been encoded," not an encoded PCI bus transaction. (Ex. Q at 14, 15 n.4 ('873 Final Written Decision) (emphasis in original); *see also* Ex. R at 14-15 ('814 Final Written Decision).

Finally, the Court will note EMC's positions here, requiring communication of "all address, data, and control bits, without discarding any of those bits" stands in sharp contrast to its position before the PTAB and Federal Circuit. (Op. Br. Ex. 7 at 12, D.I. 185 ("it would have been obvious to transmit at least *some* of the PIC address bits…") (emphasis added); *see also* Op. Br. Ex. 8 at 11-12, D.I. 185 (same); Ex. EE at 25, 29, 35-36 (EMC Appeal Brief); Ex. FF at 14 (only some address bits are required to meet the communicating limitation) (EMC Appeal Reply).) EMC's proposed construction lacks intrinsic support, contradicts the language of several claims, is technically incorrect, and contradicts its own PTAB and Federal Circuit arguments. It should be rejected.

VII. CONCLUSION

For the reasons set forth above, EMC has shown no reason to deviate from the prior constructions of Judge Davis and the PTAB. Nor has EMC presented evidence establishing a clear and unequivocal disavowal that would narrow the claims as EMC urges. Nothing that occurred before the PTAB is disavowal, let alone the specific disavowal be required to modify Judge Davis's constructions. To the contrary, the events of the PTAB proceedings fully support those constructions.

Dated: February 13, 2017

Respectfully submitted,

/s/ James Brogan

James P. Brogan *(pro hac vice)*
COOLEY LLP
380 Interlocken Crescent, Ste. 900
Broomfield, CO 80021-8023
Telephone: (720) 566-4000
Facsimile: (720) 566-4099
jbrogan@cooley.com

Thomas J. Friel, Jr.
COOLEY LLP
101 California Street, 5th Floor
San Francisco, CA 94111-5800
Telephone: (415) 693-2000
Facsimile: (415) 693-2222
tfriel@cooley.com

Adam Gershenson (BBO # 671296)
COOLEY LLP
500 Boylston Street
14th Floor
Boston, MA 02116-3736
Telephone: (617) 937-2379
Facsimile: (617) 937-2400
agershenson@cooley.com

ATTORNEYS FOR PLAINTIFF ACQIS LLC

CERTIFICATE OF SERVICE

I hereby certify that this document filed through the CM/ECF system will be sent electronically to the registered participants as identified on the Notice of Electronic Filing (NEF) and paper copies will be sent to those indicated as non-registered participants on February 13, 2017.

/s/ James Brogan

141227537 v15